CLAIMS

What is claimed is:

1. A routing element for use in a semiconductor device assembly, comprising:

a polymeric film; and

at least one conductive trace including first and second portions carried adjacent opposite sides of said polymeric film, said at least one conductive trace located so as to facilitate electrical connection between remote first and second locations of the semiconductor device assembly.

2. The routing element of claim 1, further comprising:

a contact pad located at each end of said at least one conductive trace.

3. The routing element of claim 2, wherein said contacts are located on opposite sides of said polymeric film from one another.

4. The routing element of claim 1, wherein said polymeric film is substantially planar.

5. The routing element of claim 1, wherein said polymeric film is flexible.

6. The routing element of claim 1, wherein said at least one conductive trace extends from a first location proximate a first edge of said polymeric film to a second location proximate an opposite, second edge of said polymeric film.

7. The routing element of claim 1, wherein said polymeric film carries a plurality of conductive traces.

8. The routing element of claim 1, wherein at least a portion of said at least one conductive trace is carried internally within said polymeric film.

9. The routing element of claim 1, wherein an electrically conductive via that extends at least partially through said polymeric film electrically connects said first and second portions.

10. A semiconductor device assembly comprising:

a substrate;

at least one semiconductor device secured to said substrate; and

a polymeric film positioned at least partially over at least one of said substrate and said at least one semiconductor device, said polymeric film carrying at least one conductive trace in communication with at least one of a terminal of said substrate and a bond pad of said at least one semiconductor device.

11. The assembly of claim 10, wherein said polymeric film is at least partially superimposed over said at least one semiconductor device.

12. The assembly of claim 11, wherein said at least one conductive trace at least partially establishes communication between a bond pad of said at least one semiconductor device and a corresponding terminal of said substrate.

13. The assembly of claim 12, wherein communication between said bond pad and said corresponding terminal is further established by at least one discrete conductive element positioned electrically between said at least one conductive trace and at least one of said bond pad and said corresponding terminal.

14. The assembly of claim 10, comprising a plurality of semiconductor devices at different locations on said substrate.

15. The assembly of claim 14, wherein said polymeric film is secured to said substrate laterally between at least two semiconductor devices of said plurality of semiconductor devices.

16. The assembly of claim 15, wherein at least one conductive trace of said plurality of conductive traces carried by said polymeric film at least partially establishes communication between a bond pad of one of said at least two semiconductor devices and a corresponding bond pad of another of said at least two semiconductor devices.

17. The assembly of claim 16, wherein said at least one conductive trace communicates with a terminal of said substrate which, in turn, communicates with said bond pad.

18. The assembly of claim 17, further comprising discrete conductive elements between said terminal and each of said at least one conductive trace and said bond pad.

19. The assembly of claim 10, wherein said substrate comprises at most four conductive layers.

20. The assembly of claim 10, wherein said plurality of conductive traces of said polymeric film provide a more direct electrical route between than any conductive trace carried by said substrate.

21. The assembly of claim 16, wherein another bond pad of said one semiconductor device is in communication with at least a terminal of said substrate by way of another conductive trace carried by said polymeric film.

22. The assembly of claim 10, wherein said polymeric film and said at least one conductive trace extend through a plane of said substrate.

23. The assembly of claim 22, wherein opposite ends of said at least one conductive trace are electrically exposed at opposite sides of said polymeric film.

24. The assembly of claim 22, wherein opposite ends of said at least one conductive trace are electrically exposed at the same side of said polymeric film.

25. A carrier for at least one semiconductor device, comprising:
a substrate carrying at least one terminal and at least one conductive trace; and
a polymeric film positioned at least partially over said substrate and carrying at least one additional conductive trace.

26. The carrier of claim 25, wherein said substrate comprises at most four conductive layers.

27. The carrier of claim 25, wherein said polymeric film is at least partially adhered to said substrate.

28. The carrier of claim 27, wherein said at least one additional conductive trace at least partially establishes communication between said at least one terminal and another terminal carried upon said substrate.

29. The carrier of claim 28, wherein communication between said at least one terminal and said another terminals is further established by way of at least one discrete conductive element that electrically connects said at least one additional conductive trace to at least one of said at least one terminal and said another terminal.

30. The carrier of claim 25, wherein said polymeric film is configured to be disposed at least partially over the at least one semiconductor device carried by said substrate.

31. The carrier of claim 25, wherein said at least one additional conductive trace carried upon said polymeric film is configured to at least partially establish communication

between said at least one terminal and a corresponding bond pad of the at least one semiconductor device.

32. The carrier of claim 31, wherein communication between said at least one terminal and said corresponding bond pad is further established by way of at least one discrete conductive element electrically connecting said at least one additional conductive trace to at least one of said at least one terminal and said corresponding bond pad.

33. The carrier of claim 31, wherein said at least one additional conductive trace carried upon said polymeric film is configured to at least partially establish communication between a bond pad of the at least one semiconductor device and a corresponding bond pad of at least another semiconductor device carried by said substrate.

34. The carrier of claim 33, wherein communication between said bond pad and said corresponding bond pad is further established by way of at least one discrete conductive element electrically connecting said at least one additional conductive trace and at least one of said bond pad and said corresponding bond pad.

35. The carrier of claim 25, wherein said substrate includes at least one aperture formed therethrough for receiving a portion of said polymeric film and said at least one additional conductive trace to facilitate positioning of different portions of said polymeric film over portions of opposite sides of said substrate.

36. The carrier of claim 35, wherein opposite ends of said at least one additional conductive trace are electrically exposed at opposite sides of said polymeric film.

37. The carrier of claim 35, wherein opposite ends of said at least one additional conductive trace are electrically exposed at the same side of said polymeric film.

38. A method for designing a routing element for use in a semiconductor device assembly, comprising:

configuring a polymeric film to be disposed between at least two areas of at least one of a substrate and a semiconductor device; and

configuring at least one conductive trace to be carried by said polymeric film and to extend substantially between locations of said polymeric film adjacent to said at least two areas upon said disposition of said polymeric film.

39. The method of claim 38, wherein said configuring said polymeric film comprises configuring said polymeric film to electrically insulate at least portions of said at least one conductive trace.

40. The method of claim 38, wherein said configuring said at least one conductive trace comprises configuring said at least one conductive trace to be at least partially carried internally within said polymeric film.

41. The method of claim 38, wherein said configuring said at least one conductive trace comprises configuring said at least one conductive trace to extend substantially between a first contact area and a second contact area.

42. The method of claim 38, wherein said configuring said at least one conductive trace comprises configuring a plurality of conductive traces.

43. The method of claim 42, wherein said configuring said plurality of conductive traces comprises configuring positions of each of said plurality of conductive traces so as to minimize electrical interference between conductive traces of said plurality.

44. The method of claim 38, wherein said configuring said at least one conductive trace comprises configuring a position of said at least one conductive trace to extend substantially directly between said at least two areas.

45. A method for establishing electrical connections in a semiconductor device, comprising:

providing a substrate including at least one first contact area and at least one remote, unconnected, corresponding second contact area;

positioning at least one routing element carrying at least one conductive trace between said at least one first contact area and said at least one second area with ends of said at least one conductive trace extending proximate said at least one first contact area and said at least one second contact area; and

electrically connecting said at least one conductive trace between said at least one first contact area and said at least one second contact area.

46. The method of claim 45, wherein said providing comprises providing at least one semiconductor device on said substrate, said at least one semiconductor device comprising at least one of said at least one first contact area and said at least one second contact area.

47. The method of claim 46, wherein said positioning comprises positioning said at least one routing element at least partially over said at least one semiconductor device.

48. The method of claim 46, wherein said positioning comprises positioning said at least one routing element laterally adjacent to said at least one semiconductor device.

49. The method of claim 45, wherein said positioning comprises positioning said at least one routing element adjacent to conductive traces carried by said substrate with said at least one conductive trace of said at least one routing element electrically isolated from said conductive traces carried by said substrate.

50. The method of claim 45, wherein said electrically connecting comprises electrically connecting comprises disposing a discrete conductive element between said at least one conductive trace and each of said at least one first contact area and said at least one second contact area.

51. The method of claim 45, wherein said positioning comprises extending a portion of said at least one rerouting element through a plane of said substrate to locate a first end of said at least one conductive trace proximate said at least one first contact area and a second end of said at least one conductive trace proximate said at least one second contact area, located on an opposite side of said substrate from said at least one first contact area.

52 A method for designing a carrier, comprising:
configuring a substrate;
configuring at least one region on said substrate to receive a semiconductor device;
configuring a first plurality of conductive traces to be carried by said substrate; and
configuring at least one routing element to carry a second plurality of conductive traces, said routing element to be assembled with said substrate.

53. The method of claim 52, further comprising configuring terminal pads on at least one surface of said substrate.

54. The method of claim 53, wherein said configuring terminals pads comprises configuring a first plurality of terminal pads to electrically communicate with said first plurality of conductive traces.

55. The method of claim 54, wherein said configuring terminal pads further comprises configuring a second plurality of terminal pads to electrically communicate with said second plurality of conductive traces upon assembly of said at least one routing element with said substrate.

56. The method of claim 52, wherein said configuring said first plurality of conductive traces comprises configuring said first plurality of conductive traces to extend along at most four conductive layers of said substrate.

57. The method of claim 52 wherein said configuring said at least one routing element comprises configuring said second plurality of conductive traces to extend to a location proximate said at least one region upon assembly of said at least one routing element with said substrate.

58. The method of claim 52, further comprising configuring an aperture through said substrate.

59. A semiconductor device assembly comprising:
a substrate carrying a first plurality of conductive traces;
a routing element carrying a second plurality of conductive traces positioned at least partially on said substrate; and
at least one semiconductor device secured to said substrate.

60. The assembly of claim 59, wherein said routing element is at least partially superimposed over said at least one semiconductor device.

61. The assembly of claim 60, wherein at least one conductive trace of said second plurality of conductive traces at least partially establishes electrical communication between a bond pad of said at least one semiconductor device and a corresponding terminal of said substrate.

62. The assembly of claim 61, wherein communication between said bond pad and said corresponding terminal is further established by at least one discrete conductive element positioned electrically between said at least one conductive trace and at least one of said bond pad and said corresponding terminal.

63. The assembly of claim 59, comprising a plurality of semiconductor devices at different locations on said substrate.

64. The assembly of claim 63, wherein said routing element is secured to said substrate laterally between at least two semiconductor devices of said plurality of semiconductor devices.

65. The assembly of claim 64, wherein at least one conductive trace of said second plurality of conductive traces at least partially establishes communication between a bond pad of one of said at least two semiconductor devices and a corresponding bond pad of another of said at least two semiconductor devices.

66. The assembly of claim 65, wherein said at least one conductive trace communicates with a terminal of said substrate which, in turn, communicates with said bond pad.

67. The assembly of claim 66, further comprising discrete conductive elements between said terminal and each of said at least one conductive trace and said bond pad.

68. The assembly of claim 59, wherein said substrate comprises at most four conductive layers.

69. The assembly of claim 58, wherein said plurality of conductive traces of said routing element provide a more direct electrical route between than any conductive trace carried by said substrate.

70. The assembly of claim 65, wherein another bond pad of said one semiconductor device is in communication with at least a terminal of said substrate by way of another conductive trace of said second plurality of conductive traces.

71. The assembly of claim 59, wherein said routing element and said at least one conductive trace extend through a plane of said substrate.

72. The assembly of claim 71, wherein opposite ends of said at least one conductive trace are electrically exposed at opposite sides of said routing element.

73. The assembly of claim 71, wherein opposite ends of said at least one conductive trace are electrically exposed at the same side of said routing element.